T O M A H A W K

Orchidée Semiconductor Layer-2 Packet Routing Engine for ISDN, X.25 and xDSL Applications.

Features

- Support for IOM, IOM-2, GCI, TDM and PCM Layer-2 backplane interfaces
- Variable timeslot PCM interface
- Timeslot interchange support between serial backplane interfaces
- Parameterized number of HDLC's with parameterized FIFO depths
- Full LAPB and LAPD procedures support
- X.25 and ISO3309 support
- HDLC transparent mode for non-encapsulated voice CODEC data
- CRC16, CRC32 and ISO CRC16 support
- Pin direction reversal and TIC bus support
- Master and Slave mode support at all interfaces
- NT and TE mode support
- Synchronous, memory-mapped external data bus

Description

The Orchidée Semiconductor Tomahawk module is a general purpose packet data router which accepts a full-duplex Time Division Multiplexed (TDM) layer-1 serial data stream, performs layer-2 data processing and inputs/outputs parallel formatted octets for subsequent layer-3 handling by a host CPU. Supported standards at the Tomahawk backplane interfaces are IOM, IOM-2, GCI, PCM and Lucent TDM bus. Layer-2 processing is performed by integrated HDLC's which satisfy all requirements of the ISO/IEC-3309 LAPD and LAPB procedures. The HDLC's include parameterized transmit and receive fifo's for data buffering at the 8-bit CPU interface.

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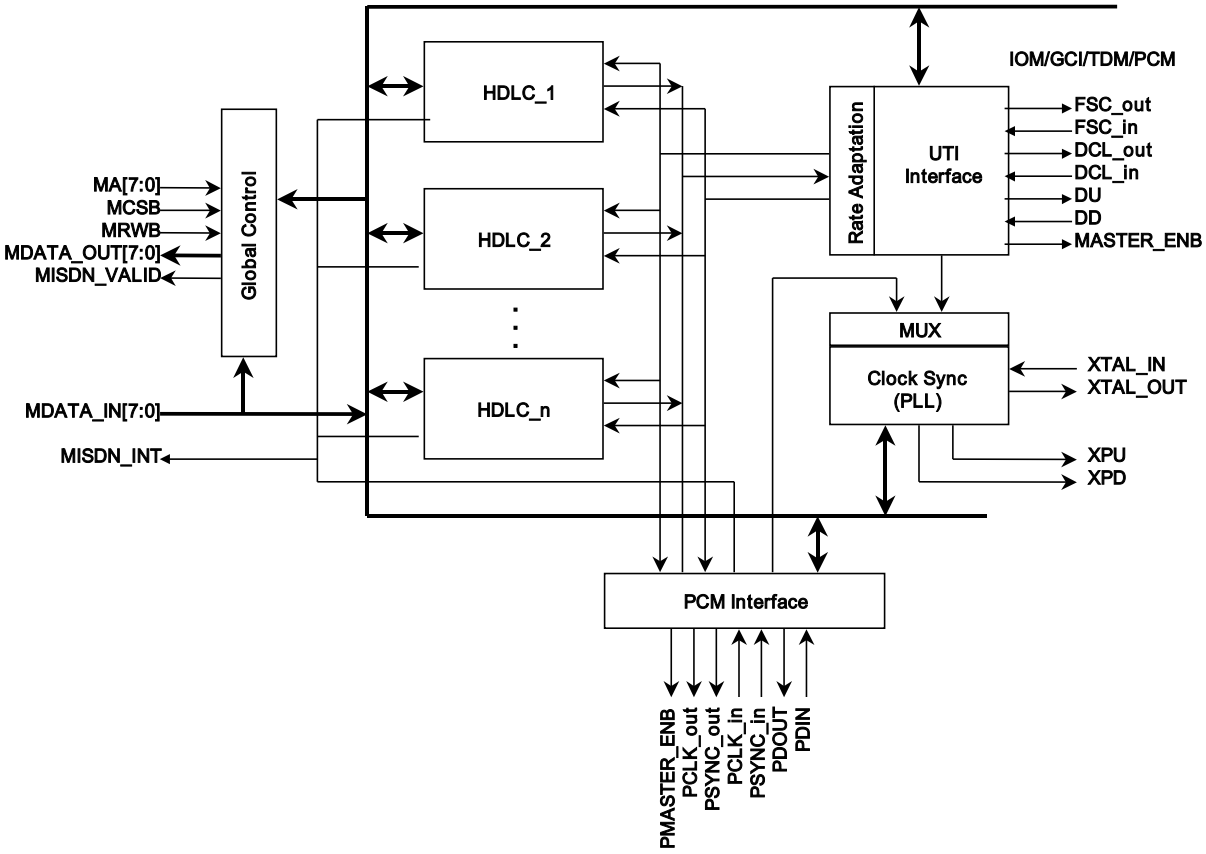
Block Diagram



Pin Description

Pin	Type	**I/F**	Function
RSTB	Input	All	Active low asynchronous reset signal.
XTAL1	Input	Clock	High frequency oscillator input.
XTAL_CLK_out	Output	Clock	DCL-locked clock output.
XTAL_CLK_in	Input	Clock	DCL-locked clock input.
MDATA_IN[7:0]	Input	MPU	MPU data input bus.
MDATA_OUT[7:0]	Output	MPU	MPU data output bus.
MA[7:0]	Input	MPU	MPU Input register address.
MRWB	Input	MPU	MPU Read/Write Not signal.
MCSB	Input	MPU	MPU active low chip select signal.
MISDN_VALID	Output	MPU	Indicates valid data present on the MDATA_OUT bus.
MISDN_INT	Output	MPU	Logical “OR” of all ISR interrupts.
SDS1	Output	UTI	B1/B2 IOM-2 Channel_0 Select
SDS2	Output	UTI	IC1/IC2 IOM-2 Channel_1 Select
BCL	Output	UTI	IOM-2 Bit Clock
UFSC_out	Output	UTI	UTI Interface frame synch signal output.
UFSC_in	Input	UTI	UTI Interface frame synch signal input.
UDCL_out	Output	UTI	UTI Interface data clock signal output.
UDCL_in	Input	UTI	UTI Interface data clock signal input.
UMASTER_ENB	Output	UTI	Active low UTI FSC/DCL enable signal. Low when UTI is in master mode.
UDout	Output	UTI	UTI Interface data output
UDin	Input	UTI	UTI Interface data input
UDout_reverse	Output	UTI	UTI Interface data output (reverse direction)
UDin_reverse	Input	UTI	UTI Interface data input (reverse direction)
PCM_TIMESLOT[4:0]	Output	PCM	Active PCM Octet (timeslot)
PMASTER_ENB	Output	PCM	Active low PCM FSC/PCLK enable signal. Low when PCM is in master mode.
PDout	Output	PCM	PCM Interface serial data output
PDin	Input	PCM	PCM Interface serial data input
PSYNC_out	Output	PCM	PCM Interface frame synch output signal
PCLK_out	Output	PCM	PCM MASTER output clock
PSYNC_in	Input	PCM	PCM Interface frame synch input signal
PCLK_in	Input	PCM	PCM SLAVE input clock

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